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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,712	03/31/2004	George W. Conner	T0529.70017US00	7399

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EXAMINER	
BARAN, MARY C	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/813,712	CONNER, GEORGE W.	
	Examiner	Art Unit	
	Mary Kate B. Baran	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 28 June 2004 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because a copy of the information disclosure statement was not received. It has not been placed in the application file, and the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Specification

2. The disclosure is objected to because of the following informalities:

(a) On page 1 line 12, "used identify" should be – used to identify –.

(b) On page 2 line 5, "S_{in-}" should be – S_{in-}. –.

(c) On page 4 line 1, "measurements is" should be – measurement is –.

(d) On page 6 line 5, "A a" should be – A –.

Appropriate correction is required.

Claim Objections

3. Claims 3 and 18 are objected to because of the following informalities:

(a) Claim 3 page 14 line 21, "level" should be – levels –.

(b) Claim 18 page 17 line 10, "component," should be – component. –.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 provides for the use of differential signals to analyze the performance of the semiconductor component, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass.

What about all the limitations in the parent claim?

Claim 12 provides for the use of parameters of the differential signal to adjust the manufacturing process, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass.

A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Same question

Claim Rejections - 35 USC § 101

5. Claims 11-13 are rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under

35 U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and *Clinical Products, Ltd.* v. *Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 7, 8, 10, 14-18 and 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Patel (U.S. Patent No. 6,759,864).

Referring to claim 1, Patel teaches a method of performing a measurement on a differential signal (see Patel, column 4 lines 3-5), comprising: providing each leg of the differential signal to an input of a comparator having at least a first and second input (see Patel, column 4 lines 5-11); introducing a plurality of bias levels into the comparison, whereby the output of the comparator is a first logical value when the value at the first input exceeds the value at the second input by the bias level (see Patel, column 6 lines 1-7); taking a plurality of sets of samples of the output of the comparator, with a set of samples for each of the bias levels, each of the samples in each of the sets correlated in time to a point on the waveform (see Patel, column 8 lines 12-18 and lines 30-36); selecting a set of samples having values with a predetermined percentage of a

predetermined logical value (see Patel, column 8 lines 36-48 and Figure 12); and associating the bias value used to take the samples in the selected set with the value of the differential signal at the point on the waveform (see Patel, column 8 lines 48-60).

Referring to claim 2, Patel teaches that introducing a bias level comprises passing a current through a resistor connected to one of the first and second inputs of the comparator (see Patel, Figure 5).

Referring to claim 4, Patel teaches that the comparator is contained inside a commercially available component having leads accessible at its exterior, including exterior leads coupled to the first and second inputs of the comparator (see Patel, Figure 1).

Referring to claim 5, Patel teaches that the resistor is coupled to the input of the comparator (see Patel, column 6 lines 16-18).

Referring to claim 6, Patel teaches that each leg of the differential signal is AC coupled to one of the first and second inputs to the comparator (see Patel, Figure 1).

Referring to claim 7, Patel teaches that introducing a bias level comprises altering the operating characteristics of the comparator (see Patel, column 4 lines 29-33).

Referring to claim 8, Patel teaches that the comparator is contained inside a commercially available component having leads accessible at its exterior, including exterior leads coupled to the fist and second inputs of the comparator and introducing a bias level comprises applying an electrical signal to at least one of the leads coupled to the first and second inputs of the comparator (see Patel, column 4 lines 2-10).

Referring to claim 10, Patel teaches a method of manufacturing a semiconductor component incorporating the method of claim 1 wherein the differential signal is an output of the semiconductor component at a stage in its manufacture (see Patel, column 4 lines 21-23) and steps of claim 1 are repeated to associate values with a plurality of points on the differential signal (see Patel, column 4 lines 25-35).

Referring to claim 14, Patel teaches an automatic test system suitable for making measurements of a differential signal applied as an input to the test system, the test system having a measurement circuit (see Patel, column 4 lines 2-4) comprising: a comparator having: a first and second signal input terminals (see Patel, column 4 lines 4-10); an output providing a logical signal indicating the results of a comparison (see Patel, column 4 lines 41-50); and a timing input controlling the time at which a comparison is made (see Patel, column 7 lines 53-60); means for biasing the comparison by a variable amount in response to a control signal (see Patel, column 6 lines 1-7); control circuitry providing a timing signal connected to the timing input of the

comparator (see Patel, column 7 lines 53-60) and a control signal to the means for biasing (see Patel, column 7 line 66 – column 8 line 6); and data analysis circuitry having an input coupled to the output of the comparator, the data analysis circuitry determining parameters of the differential signal from the output of the comparator (see Patel, column 4 lines 25-50).

Referring to claim 15, Patel teaches that the input terminals of the comparator are AC coupled to the input of the test system and the means for biasing the comparison comprises at least one voltage source coupled to at least one of the first and second input terminals of the comparator (see Patel, column 4 lines 38-46).

Referring to claim 16, Patel teaches that the voltage source comprises a current source and a resistor with the resistor connected to the current source and an input terminal of the comparator (see Patel, column 4 lines 11-24).

Referring to claim 17, Patel teaches that the comparator is enclosed in semiconductor packaging with the first and second input terminals accessible through leads on the outside of the package (see Patel, column 4 lines 19-24).

Referring to claim 18, Patel teaches that the comparator is part of a commercially available semiconductor component (see Patel, column 3 liens 10-14).

Referring to claim 21, Patel teaches that the comparator is a portion of an instrument installed in the automatic test system (see Patel, column 4 lines 21-24).

Referring to claim 22, Patel teaches that the test system includes the timing generator and the control circuitry comprises the timing generator (see Patel, column 7 lines 53-60).

Referring to claim 23, Patel teaches that the data analysis circuit comprises a general purpose computer programmed to determine parameters of the differential signal (see Patel, column 8 lines 44-60).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Patent No. 6,759,864) in view of Hamaoui (U.S. Patent No. 4,053,844).

Referring to claim 3, Patel teaches all the features of the claimed invention except passing a first current through a first resistor connected to the first input of the comparator and passing a second current through a second resistor connected to the

second input of the comparator, with the plurality of bias levels introduced by altering the relative level of the first current and the second current.

Hamaoui teaches passing a first current through a first resistor connected to the first input of the comparator and passing a second current through a second resistor connected to the second input of the comparator (see Hamaoui, Figure 4), with the plurality of bias levels introduced by altering the relative level of the first current and the second current (see Hamaoui, column 8 lines 12-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel to include the teachings of Hamaoui because connecting resistors to the first and second inputs of the comparator would have allowed the skilled artisan to limit the current entering the comparator, and determine the voltage difference at the output (see Hamaoui, column 10 lines 6-15).

Referring to claim 9, Patel teaches all the features of the claimed invention except setting strobe times at which the comparator takes samples to be at a predetermined time relative to the start of a rising edge.

Hamaoui teaches setting strobe times at which the comparator takes samples to be at a predetermined time relative to the start of a rising edge (see Hamaoui, column 5 lines 52-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel to include the teachings of Hamaoui because a

strobe would have allowed the skilled artisan to activate address locations in memory for binning (see Hamaoui, column 5 lines 56-60).

8. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Patent No. 6,759,864) in view of Variyam et al. (U.S. Patent No. 6,865,500) (hereinafter Variyam).

Referring to claim 11, Patel teaches all the features of the claimed invention except that the values associated with the plurality of points on the differential signals analyze the performance of the semiconductor component and subsequent steps in the manufacturing process of the semiconductor component are selected in response to the analysis.

Variyam teaches that the values associated with the plurality of points on the differential signals analyze the performance of the semiconductor component and subsequent steps in the manufacturing process of the semiconductor component are selected in response to the analysis (see Variyam, column 3 line 62 – column 4 line 5).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel to include the teachings of Variyam because analyzing the performance of the device under test in association with the process would have allowed the skilled artisan to determine the changes in manufacturing which alter the performance so that the defective nature of the circuit can be identified (see Variyam, column 5 lines 41-48).

Referring to claim 12, Patel teaches a process of making semiconductor devices using the method of claim 1, the process comprising: connecting a semiconductor device under test to a test system (see Patel, column 4 lines 21-23); stimulating the device under test with signals from the test system (see Patel, column 4 lines 16-19); providing a differential signal generated by the device under test to the test system and performing, with the test system, the steps of claim 1 to provide parameters of the differential signal (see Patel, column 4 lines 2-10), but does not teach using the parameters of the differential signal to adjust the manufacturing process for making semiconductor devices.

Variyam teaches using the parameters of the differential signal to adjust the manufacturing process for making semiconductor devices (see Variyam, column 9 line 53 – column 10 line 15).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel to include the teachings of Variyam because adjusting the manufacturing process based on the associated parameters would have allowed the skilled artisan to locate where in the manufacturing process the error occurs, and prevent error from occurring on subsequent chips.

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Patent No. 6,759,864) in view of Variyam et al. (U.S. Patent No. 6,865,500) (hereinafter Variyam) and further in view of Hamaoui (U.S. Patent No. 4,053,844).

Referring to claim 13, Patel and Variyam teach all the features of the claimed invention except speed binning the device under test.

Hamaoui teaches speed binning the device under test (see Hamaoui, column 4 lines 16-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel and Variyam to include the teachings of Hamaoui because speed binning would have allowed the skilled artisan to store and classify data for data checking (see Hamaoui, column 1 line 67 – column 2 line 12).

10. Claims 19, 20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patel (U.S. Patent No. 6,759,864) in view of Goergen (U.S. Patent No. 6,812,803).

Referring to claim 19, Patel teaches all the features of the claimed invention except that the semiconductor component is a differential receiver.

Goergen teaches that the semiconductor component is a differential receiver (see Goergen, column 13 lines 37-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel to include the teachings of Goergen because testing a differential receiver would have allowed the skilled artisan to determine reliable communication (see Goergen, column 2 lines 1-7).

Referring to claim 20, Patel teaches all the features of the claimed invention except that the semiconductor component is a gigabit receiver.

Goergen teaches that the semiconductor component is a gigabit receiver (see Goergen, column 3 lines 50-55).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel to include the teachings of Goergen because testing a gigabit receiver would have allowed the skilled artisan to (see Goergen, column 2 lines 1-7).

Referring to claim 24, Patel teaches all the features of the claimed invention except a user interface through which the eye pattern of the differential signal is displayed.

Goergen teaches a user interface through which the eye pattern of the differential signal is displayed (see Goergen, column 13 lines 37-48).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Patel to include the teachings of Goergen because displaying and eye pattern would have allowed the skilled artisan to examine the effect of matching the response of thru-holes and differential pairs (see Goergen, column 34-36).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(a) Shuholm teaches a circuit for processing a digital data signal.

(b) Honma teaches an optical information reproducing apparatus with a threshold level generator to eliminate DC level fluctuation.

(c) Laletin teaches a controller for generating a periodic signal with an adjustable duty cycle.

(d) Warburton et al. teach a method and apparatus for improving resolution in spectrometers processing output steps from non-ideal signal sources.

(e) Kuyel teaches a method and system for measuring jitter.

(f) Blades teaches a method and apparatus for detecting arcing in AC power systems by monitoring high frequency noise.

(g) Sechi et al. teach a computer-based real-time transient pulse monitoring system and method.

(h) Tsui et al teach a simultaneous signal detection for IFM receivers by transient detection.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B. Baran whose telephone number is (571) 272-2211. The examiner can normally be reached on Monday - Friday from 9:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6 August 2005
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